Total pages: 02

PG
MCA Semester- II Examination, 2025
MASTER OF COMPUTER APPLICATIONS
PAPER: MCA 201
(ADVANCED COMPUTER ARCHITECTURE)

Full Marks: 100 **Time: 3 Hours**

The figures in the right-hand margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

Group-A

Answer any **FIVE** of the following questions: **2×5=10**

1. Write the difference between synchronous and asynchronous pipeline.
2. Compare write through and write back policy.
3. Distinguish between logical and arithmetic shift operation.
4. What is MIPS?
5. What is IO driver?
6. State locality of reference.
7. Write the difference linear and nonlinear pipeline.
8. What is a superscalar processor?

Group-B

Answer any **FOUR** of the following questions: **15×4=60**

9. (a) Explain the terms speed, efficiency and throughput.
   (b) Derive the speedup of n-stage pipeline unit.
   (c) Consider a 4-stage pipeline processor with duration of 40ns, 45ns, 40ns and 45ns with buffer time 5ns. Calculate speedup, efficiency and throughput for 100 instructions. 6+4+(2+2+1)
10. (a) With proper diagram discuss 4-level hierarchical memory organization.
    (b) Compare among temporal, special and sequential locality of references.
    (c) What is inclusion property of memory hierarchy? Explain two policies to maintain coherence property of memory hierarchy. 6+3+(3+3)
11. (a) What is cache memory? How can we obtain hit ratio and miss ratio?
    (b) Write advantages and disadvantages of virtual memory.
    (c) Consider Reference String
    7,0,1,2,3,0,2,3,4,5,7,1,0,2,1
    Calculate hit ratio using Optimal page replacement policy. 6+4+5

(P.T.O.)

12. Consider following reservation table of a nonlinear pipeline processor for function X.

<- clock ->

Stage		1	2	3	4	5	6	7	8
	S1	X					X		X
	S2		X		X				
	S3			X		X		X	

a) Find out all permissible and forbidden latencies.

b) Obtain the initial collision vector.

c) Draw state transition diagram.

d) List all simple and greedy cycle.

e) Calculate minimum average latency. 4+2+5+2+2

13. (a) What is Von Neuman Architecture? What is its limitation?
(b) Explain hardware control unit with diagram.
(c) What is I/O interface? How does central computer system connected with peripherals? Explain with diagram.
(d) Discuss about programmed I/O mode of data transfer. 3+4+4+4

14. (a) Draw and explain SIMD architecture.
(b) What is UMA model of multiprocessor? Discuss with proper diagram.
(c) Compare UMA, NUMA and COMA model of multiprocessor. 6+5+4

15. Elaborate instruction-level parallelism (ILP). Explain superscalar, supper pipelined and VLIW processor architectures with suitable examples. 6+(3+3+3)

16. Write a short note on following topic (any three) 3×5
(a) Associative mapping technique of cache memory
(b) DMA
(c) Paging
(d) Data hazard

(Internal Assessment: 30 Marks)

<<<>>>