

2023

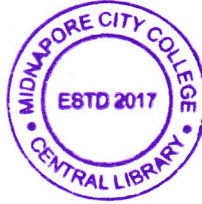
BCA 2nd Semester Examination

Digital Logic Design

PAPER — CC3T

Full Marks : 50

Time : 2 hours



The figures in the right-hand margin indicate marks.

*Candidates are required to give their answers
in their own words as far as practicable.*

Illustrate the answers wherever necessary.

Answer from **all** the Groups as directed.

GROUP—A

1. Answer **any five** questions : $2 \times 5 = 10$

(a) Convert $(6EA9)_{16}$ into decimal.

(b) Add $(+84)$ and (-75) using 2's complement.

/494

(Turn Over)



(2)

- (c) Write the truth table of Ex-NOR gate.
- (d) Implement OR gate using NAND gates only.
- (e) Design a half-adder circuit.
- (f) Differentiate between latch and flip-flop.
- (g) Draw the circuit diagram of ring counter.
- (h) What is a parity bit generator?

GROUP—B

2. Answer any **four** questions : 5×4=20

- (a) Obtain the simplified expression in sum of products for the Boolean function : 5
 $F(A, B, C, D) = \Sigma(2, 3, 12, 13, 14, 15)$
- (b) Design a combinational circuit which converts BCD to Excess-3 code. 5
- (c) Explain the working and functions of decoders and encoders. Construct 2/4 line decoder with logic gates with enable input. 2+3=5

/494 (Continued)

(3)

- (d) Implement an odd parity generator for 3-bit using a decoder. 5
- (e) What is flip-flop? Design a J-K master-slave flip-flop circuit diagram. 5
- (f) What is counter? What are the advantages and disadvantages of ripple counter? 2+3=5

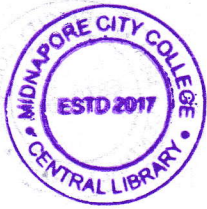
GROUP—C

3. Answer any **two** questions : 10×2=20

- (a) (i) Design a MOD-10 counter. 4+6=10
(ii) What is shift register? Design and explain a serial in parallel-out shift register.
- (b) (i) What is race around condition? How can this condition be removed? 4+6=10
(ii) Design a 16 : 1 MUX using 4 : 1 MUXs. 5+5=10
- (c) Realize a full subtractor using decoders. 10

/494 (Turn Over)





(4)

(d) Write short notes on *any two* of the following :
5×2=10

- (i) Combinational circuit
- (ii) SISO register
- (iii) ASCII Code
- (iv) Seven-segment display

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