2022

1st Semester Examination

COMPUTER SCIENCE (Honours)

Paper : C 2-T

(Computer System Architecture)

[CBCS]

Full Marks : 40 Time : Two Hours

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

Group - A

1. Answer any *five* questions : 2×5=10

(a) Represent the decimal number –0.75 in the IEEE single-precision format. 2

(b) What is the problem occurred when we perform $(1010)_2$-$(1010)_2$ using 1's complement? How to overcome this problem? 2

(c) Compare CISC and RISC. 2

(d) What are the advantages and disadvantages of micro-program control unit over hardwired control unit? 2

P.T.O.

(e) Evaluate the following arithmetic expression using one-address instruction. X = (A+B)/(C*D) 2

(f) Write the function of below mentioned registers :

MAR, SP, IR, PC 2

(g) Design EX-OR gate as an inverter. 2

(h) What will be the maximum capacity of a memory which uses an address bus of size 16 bit? 2

Group - B

Answer any *four* questions : 5×4=20

2. (a) (i) Design and explain 4-bit binary adder-subtractor unit.

(ii) What is snooping protocol? 4+1

(b) A computer has a main memory of 64K × 16 and a cache memory of 1K word. The cache uses direct mapping with a block size of four word.

(i) How many memory bits are there in the Tag, Index, Block and Word fields of the address format?

(ii) How many bits are there in each word of cache memory?

(iii) How many blocks can the cache memory accommodate? 3+1+1

(c) (i) Use Multiplexer to implement logical circuit for the below function :

$F(A, B, C, D) = \Sigma(0, 1, 2, 3, 4, 10, 11, 14, 15)$.

(ii) What are the demerits of direct cache mapping? 4+1

(d) (i) Write short note on DMA.

(ii) Draw and explain the instruction state cycle. 2+3

(e) (i) Design a full-subtractor using two half-subtractor and an OR gate.

(ii) If $\sqrt{41} = 5$, then what is the base (radix) of the number system. 4+1

(f) (i) Draw a half-adder using only NAND gate.

(ii) Write short note on Register indirect addressing mode. 3+2

Group - C

Answer any ***one*** question : 10×1=10

3. (a) (i) Reduce the expression $f = \pi M$ (2, 8, 9, 10, 11, 12, 14) using K-map and implement the real minimal expression in logic gate.

(ii) Multiply –6 and 7 using Booth's multiplication technique.

P.T.O.

(iii) A hierarchical cache-main memory subsystem has the following specifications :

- cache access time of 160 ns
- main memory access time of 960 ns
- Hit ratio of cache memory is 0.9.

Calculate the average access time and efficiency of the memory system. 3+3+4

(b) (i) What are the minimum and maximum integers representable in n-bit value using signed magnitude method, signed 1's complement method, and signed 2's complement method?

(ii) Construct 1K × 4 memory using 512 × 2 RAM chip.

(iii) How a DF/F can be converted to a J-K F/F. 3+3+4