



বিদ্যাসাগর বিশ্ববিদ্যালয়

**VIDYASAGAR UNIVERSITY**

**BCA**

**1st Semester Examination 2021**

**DIGITAL ELECTRONICS**

**PAPER—1104**

*Full Marks : 70*

*Time : 3 Hours*

*The figures in the right-hand margin indicate full marks.*

*Candidates are required to give their answers in their own words as far as practicable.*

*Illustrate the answers wherever necessary.*

**Group – A**

Answer any *four* questions.

4×15

1. (a) Implement XOR logic gate using NOR Gates.

(b) Prove that :

$$AB + C(\overline{AB + AC}) = AB$$

(c) Implement  $f(A,B,C) = \sum_m(0,2,4,6,7)$  using 4 : 1 multiplexer.

4+4+7

2. (a) Simplify the following expression using K-map method and implement the same using logic gates :

$$f = \sum(0,2,5,7,8,10,13,15)$$

(b) Minimize the following Boolean expressions using Boolean laws.

(i)  $(A + B)(A + \bar{B})$

(ii)  $ABC + A\bar{B}C + AB\bar{C}$

(5+5)+5

3. (a) What is encoder?

(b) Design a 8 X 3 Encoder and explain its operation with a truth table.

(c) What is parity generator? Design and explain 8 bit parity generator circuit.

2+6+7

4. (a) What is flip-flop? Compare level clocking and edge triggering.

(b) Design and explain a D-flipflop.

(c) What is the advantage and disadvantage of D-flip-flop?

5+6+4

5. (a) Design and explain a 4 bit ripple up counter.

(b) Design a Gray to Binary code converter.

(c) What is shift-register?

6+7+2

6. Write short notes on any *three* of the following : 3×5
- (a) Digital comparator.
  - (b) Universal gates.
  - (c) MOD-10 counter.
  - (d) J-K master slave flip-flop.
  - (e) Full adder.

7. (a) Design MOD-7 counter by D-flip flop.
- (b) Implement J-K flip flop using SR flip flop. 8+7

8. (a) Explain bidirectional shift register.
- (b) Design a 1×16 decoder using 1×4 decoders. 8+7

**Group – B**

Answer any *one* question. 1×10

9. (a) State associative and distributive law.
- (b) Distinguish between sequential and combinational circuit.
- (c) What is prime implicant? 4+4+2

10. (a) Define race around condition.
- (b) Compare between flipflop and latch.

(c) What is parity checker?

(d) What is gray code?

2+4+2+2

**(Internal Assessment : 30)**

---

Vidyasagar University