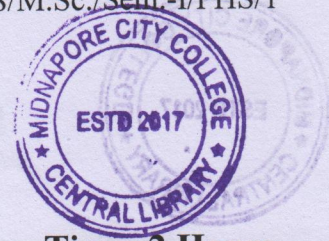


PG (NEW) CBCS
M.Sc. Semester-I Examination, 2018
PHYSICS
PAPER: PHS-104

**Full Marks: 40****Time: 2 Hours**

Write the answer for each unit in separate sheet

The figures in the right-hand margin indicate full marks.
 Candidates are required to give their answers in their own words as far as practicable.

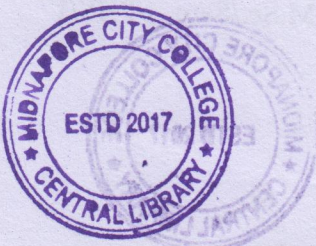
PHS 104.1: ANALOG ELECTRONICS - I

Marks: 20

Attempt Question number 1, 2 and any one from the rest.

1. Attempt any two of the following (2 × 2 = 4)
 - a. What do you mean by VSB-AM modulation and where is it used?
 - b. Explain pre-emphasis and de-emphasis in FM signal.
 - c. What is the difference between CW radar and Pulsed radar?
 - d. What is the advantage of n MOSFET over p MOSFET?
2. Attempt any two of the following (4 × 2 = 8)
 - a. Explain the detailed operation of MTI radar.
 - b. Determine the maximum range of a radar.
 - c. With necessary block diagram, explain the detailed operation of a super heterodyne AM radio receiver. What is the value of IF used in AM receivers?
 - d. Describe how you can use an OPAMP as constant current source.
3. a. Derive the expression for FM signal and hence find out the theoretical bandwidth of FM signal. (4)
 - b. Explain any method of generation of FM signal. (3)
 - c. What is the advantage of using limiter in FM receiver? (1)
4. a) What do you mean by radio horizon? (2)
 - b) What is radiation resistance of an antenna? (2)
 - c) Describe the radiation pattern of a half-wave dipole antenna. (4)

(Turn Over)



PHS 104.2: DIGITAL ELECTRONICS - I

Marks: 20

Attempt Question number 1, 2 and any one from the rest.

1. Attempt any two of the following (2 × 2 = 4)
- a. Define J-K flipflop using S-R latch.
 - b. Design a 8:1 MUX using two 4:1 MUX.
 - c. Use Karnaugh map to minimize the following logical expression

$$Y = \sum_m(0,2,4,6)$$
 - d. Convert the following circuit using NAND gate only

$$Y = (A+B).(C+D)$$
2. Attempt any two of the following (4 × 2 = 8)
- a. Design a Full Adder circuit using MUX.
 - b. Draw a binary to BCD converter.
 - c. Design 3-bit up/down ripple counter with a proper mode select line.
 - d. Explain the operation of a 4 bit SIPO register with proper circuit diagram.
4. a. Design a BCD to seven segment decoder. (4)
 b. Design a four bit binary converter using T Flip-Flop. (4)
5. a. Two signals A(A₁ A₀) and B(B₁ B₀) are applied to a digital circuit which goes high when two signals are equal. Write down the truth table and draw the circuit. (4)
 b. Give the circuit of 4 bit odd parity generator. (4)
